REMARKS

Applicant has carefully studied the outstanding Official Action. The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 20, 27-29 and 34 stand rejected under 35 USC 112, second paragraph, for failing to provide sufficient antecedent basis for all elements contained therein. Claim 20 has been amended to provide appropriate antecedent basis for all elements in these claims.

Claims 20, 28-29 stand rejected under 35 USC 102(b) as being anticipated by Yamawaki et al. Claims 22-23, 26-27 and 34 stand rejected under 35 USC 103(a) as being unpatentable over Yamawaki et al and further in view of Salatino. Claims 24, 33 and 36 stand rejected under 35 USC 103(a) as being unpatentable over Yamawaki et al and further in view of Ichikawa. Claim 37 stands rejected under 35 USC 103(a) as being unpatentable over Yamawaki et al and further in view of Nguyen et al.

Applicant expresses his appreciation to Examiner Nema O. Berezny for the courtesy of an interview which was granted to Applicants' representative, Sanford T. Colb (Reg. No. 26,856). The interview was held in the USPTO on February 25, 2004. In the interview, claims 20 and 37 were discussed vis-à-vis the prior art patents to Yamawaki (U.S. 4,894,707) and Nguyen (U.S. 6,245,595). The Interview Summary Record states, in relevant part, "Combine claims 20 and 37, plus add the circled claim element." Applicant has amended claim 20 to include the new recitations as proposed.

Support for the amendments to claim 20 can be found in Figs. 5A-5I, and in the disclosure on page 6, line 25 – page 7, line 13, inter alia. Applicant has also added new claim 38. Support for claim 38 can be found in the embodiments of Figs. 2A-2C, inter alia.

Yamawaki et al. discloses a semiconductor device with a light transparent window including a spacer. Salatino discloses a wafer level hermetically packaged integrated circuit. Ichikawa discloses a method for manufacturing surface acoustic modules. Nguyen et al. discloses a method for forming a layer of underfill encapsulant on an integrated circuit.

None of the prior art shows or suggests a method of producing a crystalline substrate based device including "providing a wafer comprising a semiconductor microstructure including a semiconductor substrate; providing a spacer at a wafer level, said spacer defining at least one cavity extending entirely therethrough; adhesively sealing to said wafer at least one transparent packaging layer and said spacer onto said semiconductor substrate over said microstructure and at least partially spaced therefrom, thereby to define at least one gap at said at least one cavity between said microstructure and said at least one packaging layer; forming a multiplicity of electrical contacts along surfaces of said at least one packaging layer which define edges of individual packaged devices; and subsequently dicing said wafer into said individual packaged devices, wherein said spacer is formed as a piece separate from said substrate" as recited in amended claim 20.

Applicant has carefully studied the remaining prior art of record herein and concludes that the invention as described and claimed in the present application is neither shown in nor suggested by the cited art.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Respectfully submitted,

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